On the Complexity of Fault Testing for Reversible Circuits

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Reversible circuits, which permute the set of input vectors, have potential applications in nanocomputing [3], low power design [1], digital signal processing [6], and quantum computing [4]. This paper shows that given a reversible circuit C and a set of wires F of C, it is NP-hard to generate a minimum complete test set for stuck-at faults on F.

A gate is reversible if the Boolean function it computes is bijective. If a reversible gate has k input and output wires, it is called a $k \times k$ gate, or a gate on k wires. A circuit is reversible if all gates are reversible and are interconnected without fanout or feedback. If a reversible circuit has n input and output wires, it is called an $n \times n$ circuit.

We shall focus our attention to detecting faults in a reversible circuit C which cause wires to be stuck-at-0 or stuck-at-1. Let $L(C)$ be the set of all possible fault locations in C. $L(C)$ consists of all input and output wires of C, and input wires to gates in C. For an $n \times n$ reversible circuit C, a test is an input vector in $\{0,1\}^n$. A set of tests that detects all faults on $F \subseteq L(C)$ is said to be complete for F. Let $S^F(C)$ be the minimum cardinality of a complete test set for F. We denote $S^F(C)$ by $S^*(C)$ if $F = L(C)$.

A k-CNOT gate is a reversible gate on $k+1$ wires. It passes some k inputs, referred to as control bits, to the outputs unchanged, and inverts the remaining input, referred to as target bit, if the control bits are all 1. The 0-CNOT gate is just an ordinary NOT gate. A CNOT gate is a k-CNOT gate for some k. Some CNOT gates are shown in Fig. 1, where a control bit and target bit are denoted by a black dot and ring-sum, respectively. A CNOT circuit is a reversible circuit consisting of only CNOT gates. Since the 2-CNOT gate can implement the NAND function, any Boolean function can be implemented by a CNOT circuit.

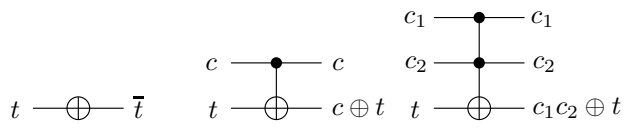
It is shown in [2] that $S^*(C) = O(\log |L(C)|)$ for any reversible circuit C. Moreover, it is shown in [5] that $S^*(C) \leq n$ if C is an $n \times n$ CNOT circuit with no 0-CNOT or 1-CNOT gates.

We show in this paper that it is NP-hard to compute $S^F(C)$ for a given CNOT circuit C and $F \subseteq L(C)$. Let MTS (Minimum Test Size) be a problem of deciding if $S^F(C) \leq B$ for a given CNOT circuit C, $F \subseteq L(C)$, and integer B. We can prove the following:

Theorem MTS *is* NP-*complete*. □

The proof of the theorem is by a reduction from SAT, a well-known NP-complete problem. We show an example of the reduction. For a Boolean function $f(x_1, x_2, x_3) = (x_1 \vee \overline{x_2} \vee x_3) \wedge (\overline{x_1} \vee \overline{x_2} \vee x_3)$, we construct a CNOT circuit $C(f)$ shown in Fig. 2, where the first and second 3-CNOT gates are corresponding to the first and second clauses of f, respectively. Let F be the set of wires numbered 1 through 17. Then we can prove that f is satisfiable if and only if $S^F(C(f)) \leq 2$. In fact, it is easy to see that f is satisfiable, and $\{(1,1,1,1,1,0,0,1),(1,1,1,1,1,1,1,0)\}$ is a complete test set for F.

The complexity of computing $S^*(C)$ for a CNOT circuit C is open.



(a) 0-CNOT gate. (b) 1-CNOT gate. (c) 2-CNOT gate.

Figure 1: CNOT gates.

References

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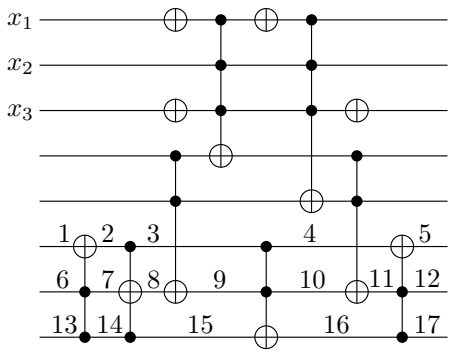

Figure 2: CNOT circuit $C(f)$ corresponding to f.